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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,489	09/18/2000	James A. McCall	10559/348001/P9836	5037

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EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2181	11

DATE MAILED: 11/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,489	MCCALL ET AL.	
	Examiner	Art Unit	
	Glenn A. Auve	2181	

-- The MAILING DATE of this communication appears on th cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,11-14 and 17-23* is/are rejected.

7)☒ Claim(s) *8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9,10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on August 4, 2003, has been entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-7,11-14, and 17-23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7,12-15,17, and 19-23 of U.S. Patent No. 6,553,450 B1 (cited by applicant). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons. The claims correspond to each other as follows:

APPLICATION	PATENT
1	1
2	2
3	3
4	4
5	5
6	6
7	7
11	12
12	13
13	14
14	1,2,5
17	15
18	17
19	19
20	20
21	21
22	22
23	23

The only differences between the claims are the inclusion of the plurality of memory ranks and interleaving the outputs of the memory ranks in the independent claims of the patent. These particular limitations are not present in the application claims. It is generally accepted that the omission of an element and its function from a device is obvious if the function of the element is

not desired [Ex parte Wu, 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989) and In re Larson, 340 F.2d 965, 144 USPQ 347 (CCPA 1965)]. Therefore in this case it would be obvious to omit the plural ranks and interleaving function as claimed in the patent in the application claims if the interleaving function is not desired.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1,2,5-7,9,11,12,14,17,19,20,22, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Lai et al., U.S. Patent Application Publication No. 2001/0052057 A1 (cited by applicant).

As per claim 1, Lai et al. (Lai) shows providing a buffer (220) in an interface between a chipset (200) and memory modules (240,260), the interface split into first and second sub-interfaces where the first sub-interface is between the chipset and buffer and the second sub-interface is between the buffer and memory modules (fig.3); and configuring the at least on buffer to properly latch the data being transferred between the chipset and the memory modules such that the sub-interfaces operate independently but in synchronization with each other (paragraphs 10-14,26, and 36-38). Lai shows all of the steps recited in claim 1.

As for claim 2, the argument for claim 1 applies. Lai also shows that the providing the at least one buffer isolates the sub-interfaces in such a manner that the sub-interfaces operate at different voltage levels (para. 10). Lai shows all of the steps recited in claim 2.

As for claim 5, the argument for claim 1 applies. Lai also shows that the providing the at least one buffer isolates the sub-interfaces in such a manner that the first sub-interface operates at higher frequency than the second (para. 12). Lai shows all of the steps recited in claim 5.

As for claim 6, the argument for claim 5 applies. Lai also shows that the first sub-interface is operated at twice the frequency of the second (para. 12). Lai shows all of the steps recited in claim 6.

As for claim 7, the argument for claim 6 applies. Lai also shows that the number of data lines in the first sub-interface is half that of the second (paragraphs 11 and 38). Lai shows all of the steps recited in claim 7.

As for claim 9, the argument for claim 1 applies. Lai also shows that the chipset is provided on a motherboard (inherent in a computer system). Lai shows all of the steps recited in claim 9.

As for claim 11, the argument for claim 1 applies. Lai also shows that each of the memory modules includes DRAM (at least in paragraph 5). Lai shows all of the steps recited in claim 11.

As for claim 12, the argument for claim 1 applies. Lai also shows that the memory modules include DDR RAM (at least in para. 5). Lai shows all of the steps recited in claim 12.

As per claims 14,17, and 20, Lai shows providing a buffer (220) in an interface between a chipset (200) and memory modules (240,260), the interface split into first and second sub-interfaces where the first sub-interface is between the chipset and buffer and the second sub-interface is between the buffer and memory modules (fig.3); and configuring the at least on

buffer to properly latch the data being transferred between the chipset and the memory modules such that the sub-interfaces operate independently but in synchronization with each other (paragraphs 10-14,26, and 36-38. Lai also shows that the providing the at least one buffer isolates the sub-interfaces in such a manner that the sub-interfaces operate at different voltage levels (para. 10). Lai also shows that the providing the at least one buffer isolates the sub-interfaces in such a manner that the first sub-interface operates at higher frequency than the second (para. 12). Lai shows all of the steps recited in claims 14,17, and 20.

As for claim 19, the argument for claim 17 applies. Lai also shows that the first sub-interface is operated at twice the frequency of the second (para. 12) and that the number of data lines in the first sub-interface is half that of the second (paragraphs 11 and 38). Lai shows all of the steps recited in claim 19.

As for claim 22, the argument for claim 20 applies. Lai also shows that the first sub-interface is operated at twice the frequency of the second (para. 12). Lai shows all of the steps recited in claim 22.

As for claim 23, the argument for claim 22 applies. Lai also shows that the number of data lines in the first sub-interface is half that of the second (paragraphs 11 and 38). Lai shows all of the steps recited in claim 23.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 3,4,18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Official Notice.

As for claim 3, the argument above for claim 2 applies. Lai does not specifically show that the operating voltage level of the first sub-interface is less than 1.0 volts. However, Official Notice is taken that the selection of specific voltage levels for specific applications is well within the level of ordinary skill in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a first sub-interface with an operating voltage of less than 1.0 volts in the system of Lai in order to ensure proper operation of the components.

As for claim 4, the argument above for claim 2 applies. Lai does not specifically show that the operating voltage level of the second sub-interface is between 1.2 and 1.8 volts. However, Official Notice is taken that the selection of specific voltage levels for specific applications is well within the level of ordinary skill in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a second sub-interface with an operating voltage of between 1.2 and 1.8 volts in the system of Lai in order to ensure proper operation of the components.

As for claim 18, the argument above for claim 17 applies. Lai does not specifically show that the operating voltage level of the first sub-interface is less than 1.0 volts and that the

operating voltage level of the second sub-interface is between 1.2 and 1.8 volts. However, Official Notice is taken that the selection of specific voltage levels for specific applications is well within the level of ordinary skill in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a first sub-interface with an operating voltage of less than 1.0 volts and a second sub-interface with an operating voltage of between 1.2 and 1.8 volts in the system of Lai in order to ensure proper operation of the components.

As for claim 21, the argument above for claim 20 applies. Lai does not specifically show that the operating voltage level of the first sub-interface is less than 1.0 volts and that the operating voltage level of the second sub-interface is between 1.2 and 1.8 volts. However, Official Notice is taken that the selection of specific voltage levels for specific applications is well within the level of ordinary skill in the art. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a first sub-interface with an operating voltage of less than 1.0 volts and a second sub-interface with an operating voltage of between 1.2 and 1.8 volts in the system of Lai in order to ensure proper operation of the components.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lai in view of Hronik et al., U.S. Pat. No. 6,381,684 B1.

As for claim 13, the argument for claim 1 applies. While Lai discusses the use of DDR DRAM as noted above with respect to claim 12, Lai does not make any mention of using QDR DRAM. However, Hronik et al. (Hronik) shows the development and use of quad data rate RAM (throughout the specification). It would have been obvious to one of ordinary skill in the art at the time of the invention to use QDR Ram as disclosed by Hronik in the system of Lai in order to provide faster memory with higher bandwidth.

Conclusion

10. Claims 8 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The IDS's filed on August 4, 2003, and September 23, 2003, have been considered.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Glenn A. Auve
Primary Examiner
Art Unit 2181

gaa
November 5, 2003